REMARKS/ARGUMENTS

Claims 1-29 are pending in this Application.

Claims 1 and 15 are currently amended. Applicants submit that support for the claim amendments can be found throughout the specification and the drawings. Claims 1-29 remain pending in the Application after entry of this Amendment. No new matter has been entered.

In the Office Action, claims 1-9 and 13-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,862,703 to Oonk (hereinafter "Oonk").

Applicants wish to thank the Examiner for the indication of allowable subject matter associated with claims 10-12.

Claim Rejections Under 35 U.S. C. § 103(a)

Applicants respectfully traverse the rejections to claims 1-9 and 13-29 and request reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) based on Oonk.

Applicants respectfully submit that a prima facie case of obviousness has not been established by the evidence presented in the Office Action. In order to establish a prima facie showing of obviousness, three requirements must be satisfied: all limitations of a pending claim must be expressly or impliedly disclosed by prior art references; there must be a suggestion or motivation in the art for the ordinarily skilled artisan to combine the limitations; and there must be a reasonable expectation of success in making such a combination. (M.P.E.P. § 2143).

Applicants respectfully submit that Oonk fails to teach or suggest at least one of the claimed limitations recited in each of the corresponding claims.

Claim 1

Amended claim 1 recites:

A method for repairing defective memory elements using self-test circuitry in a memory having a plurality of memory elements including a first memory element and a second memory element, the method comprising:

counting fails in the first memory element with an on-chip logic counter;

counting fails in the second memory element with the on-chip logic counter;

comparing the number of fails in the first memory element to the number of fails in the second memory element;

determining the one of the first memory element and the second memory element having the most fails; and

allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails.

In various embodiments, built-in self-test circuitry selectively couples memory outputs to fault detection circuitry during a self-test, thereby reducing the size of fault detection circuitry and storage required to properly test and repair a memory with multi-dimensional redundancy. (Application: Abstract). As recited in claim 1, fails in a first memory element are counted with an on-chip logic counter (emphasis added). As further recited in claim 1, fails in a second memory element are counted with the on-chip logic counter (emphasis added). As a result, the on-chip logic counter is used to allocate redundant memory elements during a self-test.

Applicants respectfully submit that Oonk fails to teach or suggest the method as recited in claim 1 for repairing defective memory elements using self-test circuitry in a memory. Instead, Oonk is directed to an external (or off-chip) memory tester that tests a memory device under test (DUT) and provides a computer with enough information to determine how to allocate replacement spare rows and columns. (Oonk: Abstract, lines 1-6). In general, memory testers are typically known to be devices external to the device under test (DUT), and are different from built-in self-test circuitry. For example, Oonk discloses that as the memory tester tests each memory cell residing at a particular address within a DUT, the memory tester writes a fail bit into a corresponding address of an error capture memory (ECM) to indicate whether the memory cell is defective. (Oonk: Summary, lines 44-48). Accordingly, Oonk requires an additional error capture memory, which is distinct from and in addition to the DUT. (Oonk: FIG. 1, DUT 12 and ECM 22). Thus, the operation of Oonk's memory tester is substantially different from repairing defective memory elements as recited in the method of claim 1 using self-test circuitry in a memory.

Applicants further submit that Oonk fails to teach or suggest counting fails in the first memory element with an on-chip logic counter and counting fails in the second memory element with the on-chip logic counter as recited in claim 1. Instead, Oonk discloses using a first

off-chip counter to count the total number of fails in a region of memory. (Oonk: FIG. 9, step 70 wherein a first level count is read). Oonk also discloses using one or more off-chip counters in addition to the first counter to count fails in second level and possibly third level regions of the region of memory tracked by the first counter. (Oonk: FIG. 9, steps 76 and 78 wherein second level and third level counts are read). Using off-chip counters in Oonk does not teach or suggest counting fails in a first memory element with an on-chip logic counter, and counting fails in a second memory element with the on-chip logic counter as recited in claim 1.

Additionally, using multiple counters for multiple regions as in Oonk does not teach or suggest counting fails in a first memory element with an on-chip logic counter, and counting fails in a second memory element with the on-chip logic counter as recited in claim 1. Moreover, in the Office Action, the Examiner acknowledges that the above-recited features for counting fails with the same counter are missing in Oonk. (Office Action dated Nov. 30, 2006: Page 3, lines 6-7).

Accordingly, the Office Action has not provided the required evidence in Oonk where all limitations of claim 1 are expressly or impliedly disclosed. For at least the reasons given above, Applicants respectfully submit that claim 1 is patentable over Oonk.

Applicants also respectfully submit that the Office Action fails to point out where in Oonk, or in the knowledge generally available to one of ordinary skill in the art, a suggestion or motivation is found to modify the memory tester in Oonk to include the on-chip logic counter recited in claim 1 to allegedly save space and reduce the cost of hardware. Applicants note that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants respectfully submit that the suggestion or motivation used in the Office Action comes from Applicants' own disclosure, and not from Oonk or the knowledge generally available to one of ordinary skill in the art. In the Application, Applicants describe in various embodiments, built-in self test circuitry that couples memory outputs to fault detection circuitry during a self-test, thereby reducing the size of fault detection circuitry and storage

required to properly test and repair a memory (and hence reducing the cost of hardware). (Application: Summary, lines 12-15; Page 10, lines 22-23).

Applicants further submit that one ordinarily skilled in the art would not make the proposed modification as alleged by the Examiner. Applicants disclose that for a stand alone memory chip, the whole memory may be tested with all of the failing locations identified by an external tester (e.g., the memory tester of Oonk). (Application: Page 3, lines 1-6). However, embedded memories may not be accessible to external memory testers. Col. 5, lines 35-60 and Col. 9, lines 18-55 of Oonk pointed to in the Office Action for allegedly providing evidence of obviousness, directly address the use of a plurality of counters in the external memory tester of Oonk. The usage of external memory testers as in Oonk is substantially different from built-in self-test circuitry.

Col. 5, lines 35-36 of Oonk disclose the external memory tester 10 that includes, among other components, a computer 14 and a set of area counters 24 that are not part of the DUT 12. Oonk further teaches that after a test is compete, more than one count from counters 24 is obtained (i.e., the counts). (Oonk: Col. 5, lines 48-50). Col. 9, lines 18-55 of Oonk disclose a portion of the processing associated with FIG. 17 of Oonk, which requires first level counters (FIG. 17, step 70; Col. 9, lines 20-25), second level counters (FIG. 17, step 79), third level counters (FIG. 17, step 78; Col. 9, lines 35-40), and fourth level counters (FIG. 17, step 86; Col. 9, lines 50-55). The portions of Oonk pointed to fail to provide any teaching or suggestion of space conservation and hardware cost reduction as alleged in the Office Action, because the external memory tester of Oonk substantially different from self-test circuitry on-chip with the device under test as the on-chip counter recited in claim 1.

Applicants further disclose that in a built-in self-test (BIST) environment it is not practical to store all of the failing locations since a large memory (e.g., the ECM of Oonk) may be required. In general, since BIST functions are ancillary to the purpose for which a chip is designed, very little space is typically allocated. (Application: Page 3, lines 7-11).

Applicants further submit that evidence of a reasonable expectation of success in making such a modification in Oonk is lacking. As discussed previously, Oonk is directed to an external memory tester, while claim 1 recites an on-chip logic counter. Applicants also note that

if the proposed modification or combination in Oonk for using single counter as recited in claim 1 would change the principle of operation of Oonk, then the teachings in Oonk are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). As illustrated in FIGS. 9 and FIGS. 17, the principle of operation in Oonk as discussed above requires the use of multiple off-chip counters in combination with an external computer, in contrast to claim 1 where fails in a first memory element are counter with an on-chip logic counter, and fails in a second memory element are counted with the on-chip logic counter.

In light of the above, Applicants respectfully submit that claim 1 is patentable over the cited references.

Claims 16 and 23

Claims 16 and 23 were rejected under similar rationale as set forth in claim 1. However, claims 16 and 23 recite claim limitations different from those present in claim 1. For example, claim 16 recites a self-test circuit that includes a multiplexer that selectively couples memory outputs to a fault counter that counts fails in each one of the plurality of memory elements tested by the self-test circuit. Claim 23 recites self-test circuitry that including a multiplexer selectively coupling an output from one of the plurality of memory elements to fault detection circuitry during a self-test.

Applicants respectfully submit that Oonk fails to teach or suggest the self-test circuit as recited in claim 16, having a multiplexer which selectively couples memory outputs to a fault counter. Applicants further respectfully submit that Oonk fails to teach or suggest the self-test circuitry as recited in claim 23, having a multiplexer selectively coupling an output from one of the plurality of memory elements to fault detection circuitry during a self-test. As discussed above, the external memory tester of Oonk is substantially different from the self-test circuitry as recited in claims 16 and 23.

FIG. 1 of Oonk clearly shows that an external computer 14 drives controller 16 to perform tests of the DUT 12. Additionally, FIG. 1 of Oonk depicts one output from the memory elements of Oonk (the data line from DUT 12 to controller 16). In FIG. 1 of Oonk, the data line is further shown as routed to comparator 20, whose output is linked via AND gate 26 to area fail

counters 24. The comparator and AND gate of Oonk are substantially different from the multiplexers as recited in claim 16 and 23, and do not teach or suggest self-test circuitry as recited in claim 16 and 23. Additionally, the static linking of comparator 20 and AND gate 26 of Oonk with the output of the memory elements fail to teach or suggest the self-test circuit as recited in claim 16, including a multiplexer which selectively couples memory outputs to a fault counter. Comparator 20 and AND gate 26 of Oonk further fail to teach to teach or suggest self-test circuitry as recited in claim 23, including a multiplexer selectively coupling an output from one of the plurality of memory elements to fault detection circuitry during a self-test.

In light of the above, Applicants respectfully submit that claims 16 and 23 are patentable over the cited references.

Claims 2-29

Applicants respectfully submit that independent claims 15, 16, and 23 are allowable for at least a similar rationale as discussed above for the allowability of claims 1, 16, and 23, and others. Applicants submit that dependent claims 2-14, 17-22, and 24-29 that depend directly and/or indirectly from the independent claims 1, 16, and 23 respectively, are also allowable for at least a similar rationale as discussed above for the allowability of the independent claims. Applicants further submit that the dependent claims recite additional features that make the dependent claims allowable for additional reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

/Sean F. Parmenter/
Sean F. Parmenter
Reg. No. 53,437

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
SFP:am
60952551 v1